HU1133

2A, High Efficiency LDS Module

FEATURES:

- High Density LDS Module
- 2A Output Current
- 95% Peak Efficiency at 5VIN
- Input Voltage Range from 2.7V to 5.5V
- Adjustable Output Voltage
- Enable / PGOOD Function
- Automatic Power Saving/PWM Mode
- Protections (UVLO, OCP: Non-latching)
- Internal Soft Start
- Compact Size: 3.0mm*3.7mm*1.2mm
- Pb-free for RoHS compliant
- MSL 2, 260C Reflow

APPLICATIONS:

- Single Li-Ion Battery-Powered Equipment
- LDOs Replacement
- Cell Phones / PDAs / Palmtops

GENERAL DESCRIPTION:

The LDS module is non-isolated dc-dc converters that can deliver up to 2A of output current. The PWM switching regulator, high frequency power inductor are integrated in one hybrid package. It only need input/output capacitors and one voltage dividing resistor.

The module has automatic operation with PWM mode and power saving mode according to loading. Other features include remote enable function, internal soft-start, non-latching over current protection, power good, and input under voltage locked-out capability.

The low profile and compact size package (3.0mm × 3.7mm x 1.2mm) is suitable for automated assembly by standard surface mount equipment. The LDS module is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE:

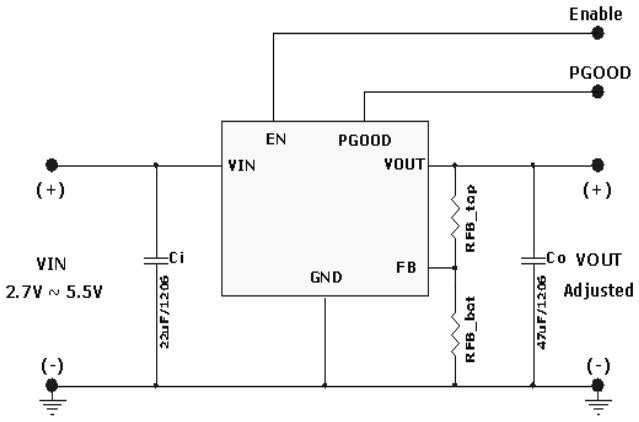

FIGURE.1 TYPICAL APPLICATION CIRCUIT

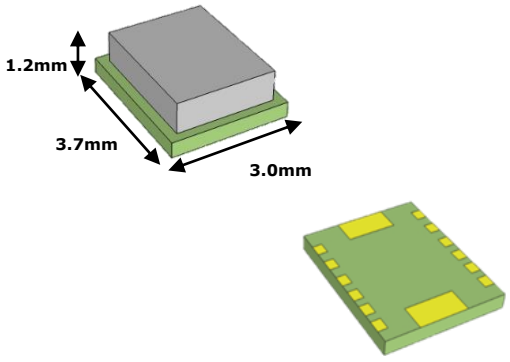

FIGURE.2 HIGH DENSITY LOW PROFILE LDS MODULE

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ELECTRICAL SPECIFICATIONS:

CAUTION: Do not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
VIN to GND		-	-	+6.0	V
VOUT to GND		-	-	+6.0	V
SW to GND	Note 1			VIN+0.3	V
EN to GND	Note 1	-	-	+6.0	V
Tc	Case Temperature of Inductor	-	-	+110	°C
Tj	Junction Temperature	-40	-	+150	°C
Tstg	Storage Temperature	-40	-	+125	°C
ESD Rating	Human Body Model (HBM)	-	-	2k	V
	Machine Model (MM)	-	-	200	V
	Charge Device Model (CDM)	-	-	500	V
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+2.7	-	+5.5	V
VOUT	Adjusted Output Voltage	0.6		+3.3	V
Ta	Ambient Temperature	-40	-	+85	°C

NOTES:
1. Parameters guaranteed and tested by power IC vendor.

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2A, High Efficiency LDS Module

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: TA = 25 ºC, Vin = 3.3V, Vout = 1.8V, Cin=22uF/X5R/6.3V , Cout=47uF/X5R/6.3V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{SD(IN)}$	Input shutdown current	Vin = 3.3V, EN = GND	-	50	-	uA
$I_{Q(IN)}$	Input supply bias current	Vin = 3.3V, Iout = 0A EN = VIN Vout = 1.8V	-	120	-	uA
$I_{S(IN)}$	Input supply current	Vin = 3.3V, EN = VIN	-	-	-	-
		Iout = 5mA Vout = 1.8V	-	3.3	-	mA
		Iout = 1.0A Vout = 1.8V	-	0.6	-	A
		Iout = 2.0A Vout = 1.8V	-	1.26	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range	Vin=3.3V, Vout=1.8V	0	-	2	A
$V_{O(SET)}$	Ouput Voltage Set Point	With 0.5% tolerance for external resistor used to set output voltage	-3.0	-	+3.0	% $V_{O(SET)}$
ΔV_{OUT} /ΔV_{IN}	Line regulation accuracy	Vin = 3.3V to 5V Vout = 1.8V, Iout = 2.0A	-	0.1	-	% $V_{O(SET)}$
ΔV_{OUT} /ΔI_{OUT}	Load regulation accuracy	Iout = 0A to 2.0A Vin = 3.3V, Vout = 1.8V	-	0.5	-	% $V_{O(SET)}$
$V_{OUT(AC)}$	Output ripple voltage	Vin = 3.3V, Vout = 1.8V EN = VIN	-	-	-	-
		IOUT = 5mA	-	25	-	mVp-p
		IOUT = 2.0A	-	10	-	mVp-p
$C_{OUT(MAX)}$	Maximum capacitive load	Iout = 2.0A, ESR≧1 mΩ	-	-	150	uF

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: TA = 25 ºC, Vin = 3.3V, Vout = 1.8V, Cin=22uF/X5R/6.3V , Cout=47uF/X5R/6.3V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Control Characteristics						
V_{EN_TH}	Enable upper threshold voltage	V_{EN_TH} rising	1.2	-	-	V
	Enable lower threshold voltage	V_{EN_TH} falling	-	-	0.4	V
F_{OSC}	Oscillator frequency	Note 1, PWM Operation	0.9	1.2	1.6	MHz
V_{REF}	Referance voltage	Note 1	-2.0%	0.600	+2.0%	V/%
V_{PGOOD_TH}	PGOOD threshold voltage	Upper trip, V_{REF} respect to the regulation, Note 1	-	+10%	-	%
		Lower trip, V_{REF} respect to the regulation, Note 1	-	-10%	-	%
V_{PGOOD_L}	PGOOD sink current capability	Sink 1mA			0.4	V
V_{PGOOD_H}	PGOOD logic high voltage	VIN=3.3V, V_{FB}=0.6V	3.2			V
■ Fault Protection						
I_{LIMIT_TH}	Current limit threshold	Peak value of inductor current, Note 1	3.2	3.8	-	A
T_{OTP}	Over temperature protection	Note 1	-	150	-	°C

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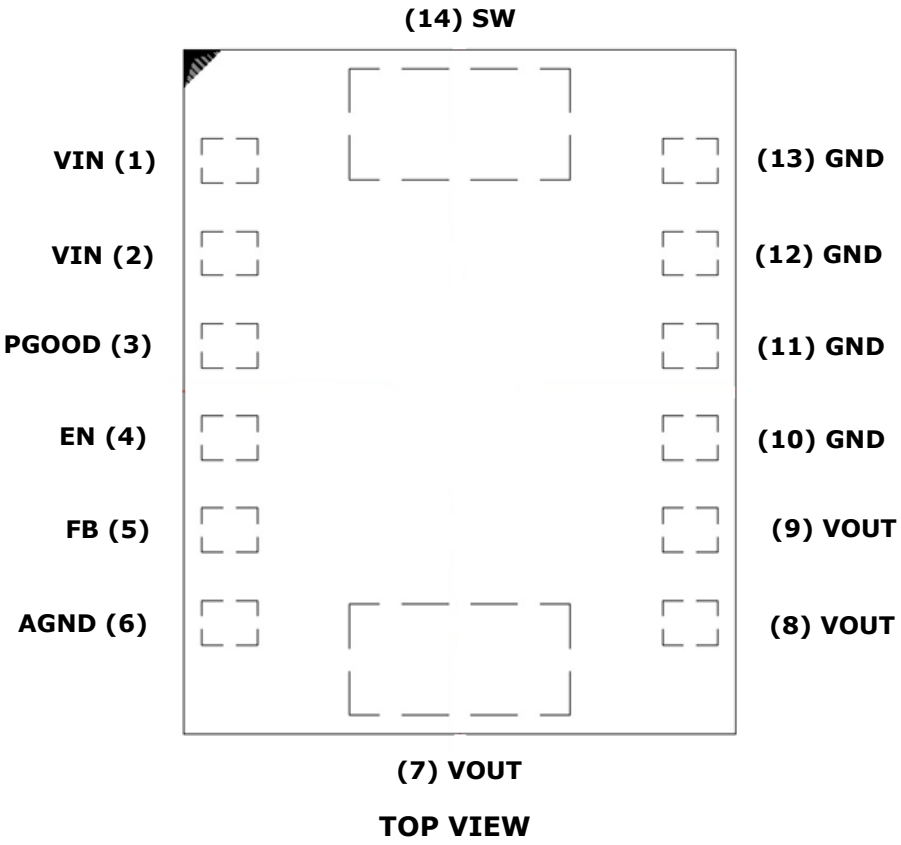
PIN CONFIGURATION:



TOP VIEW

PIN DESCRIPTION:

Symbol	Pin No.	Description
VIN	1, 2	Power input pin. It needs to connect input rail.
PGOOD	3	Power Good indicator. The pin output is an open drain that connects to VIN by an internal pull-up resistor. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level. If FB voltage is out of that regulation range, it is LOW.
EN	4	On/Off control pin for module. EN = LOW, the module is off. EN = HIGH, the module is on.
FB	5	Feedback input. Connect an external resistor divider from the output to GND to set the output voltage.
AGND	6	Analog ground.
VOUT	7, 8, 9	Power output pin. Connect to output for the load.
GND	10, 11, 12, 13	Power ground pin for signal, input, and output return path. This pin needs to connect one or more ground plane directly.
SW	14	Switch output

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2A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (1.0VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 76.2mm×76.2mm×1.6mm, 4 layers.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.

The following figures provide the typical characteristic curves at 1.0Vout.

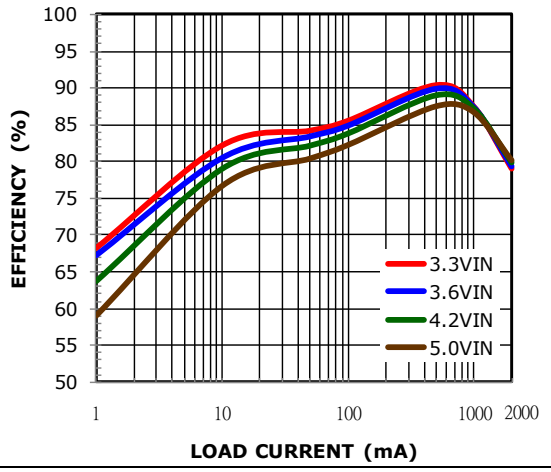

FIG.3 EFFICIENCY V.S. LOAD CURRENT

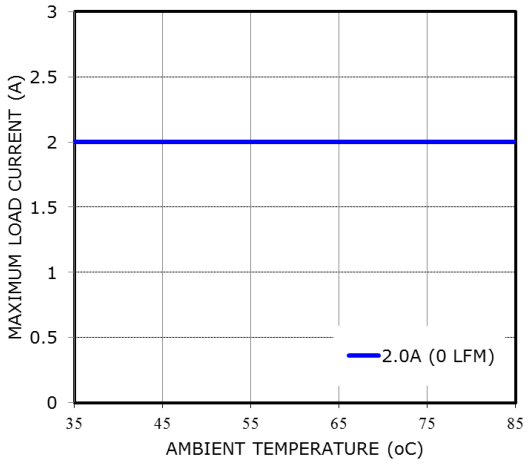

FIG.4 DE-RATING CURVE

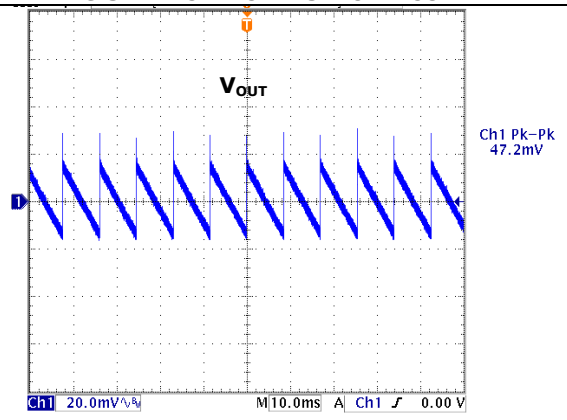

FIG.5 OUTPUT RIPPLE
(5VIN, IOUT=0A)

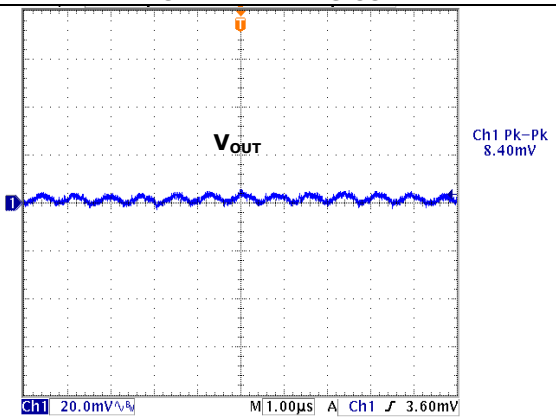

FIG.6 OUTPUT RIPPLE
(5VIN, IOUT=2A)

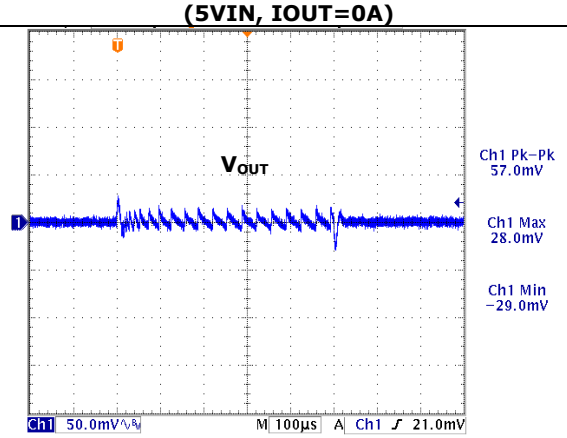

FIG.7 TRANSIENT RESPONSE
(5VIN, 0% to 100% LOAD STEP)

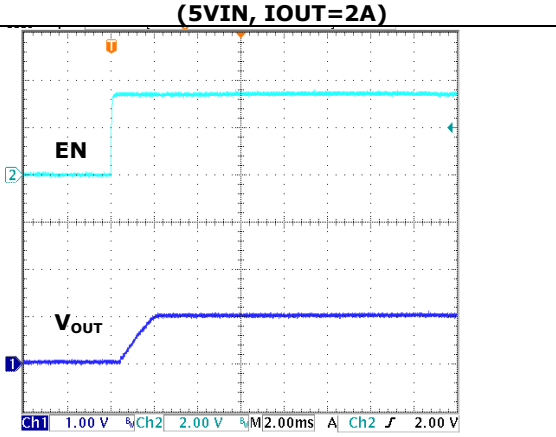

FIG.8 TURN-ON
(5VIN, IOUT=2A)

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2A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (1.2VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 76.2mm×76.2mm×1.6mm, 4 layers. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.

The following figures provide the typical characteristic curves at 1.2Vout.

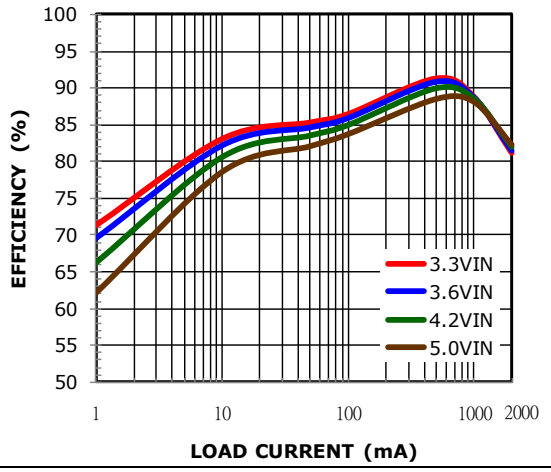

FIG.9 EFFICIENCY V.S. LOAD CURRENT

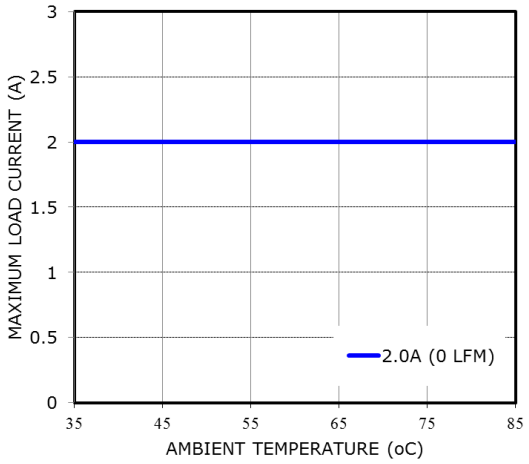

FIG.10 DE-RATING CURVE

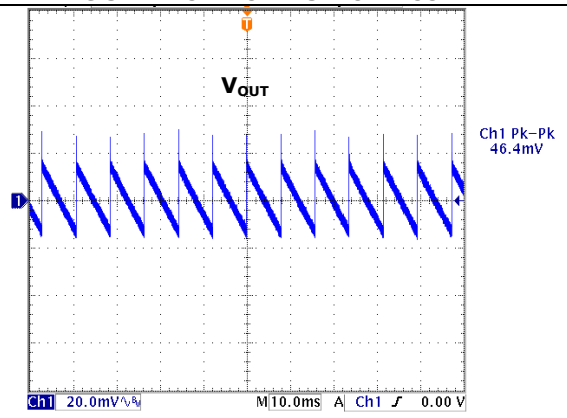

FIG.11 OUTPUT RIPPLE
(5VIN, IOUT=0A)

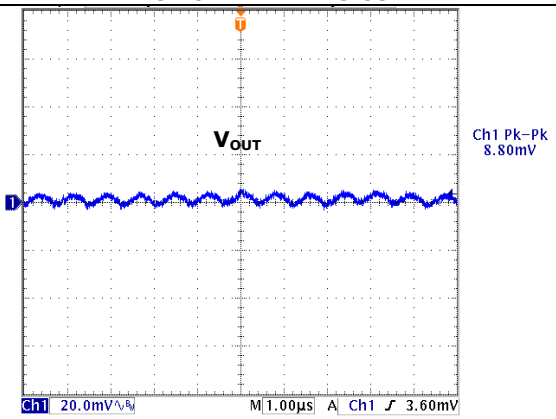

FIG.12 OUTPUT RIPPLE
(5VIN, IOUT=2A)

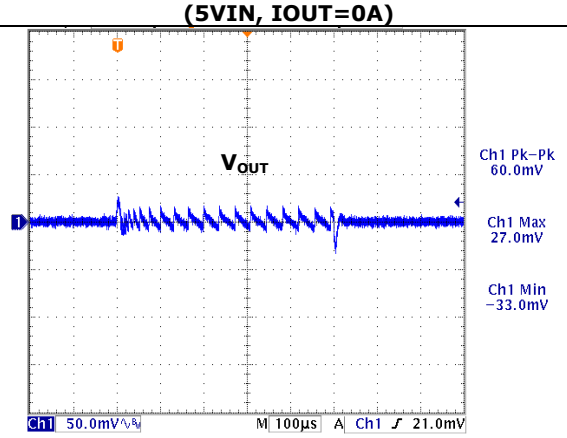

FIG.13 TRANSIENT RESPONSE
(5VIN, 0% to 100% LOAD STEP)

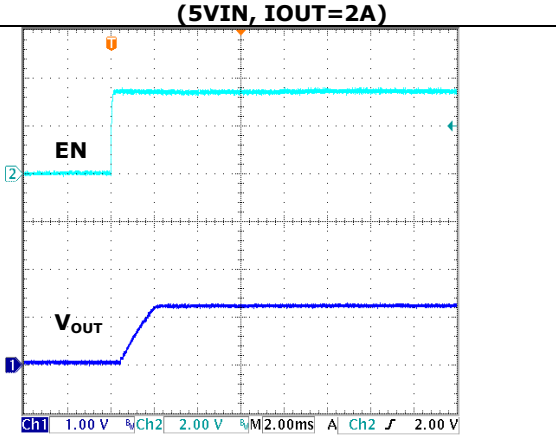

FIG.14 TURN-ON
(5VIN, IOUT=2A)

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2A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (1.8VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 76.2mm×76.2mm×1.6mm, 4 layers.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.

The following figures provide the typical characteristic curves at 1.8Vout.

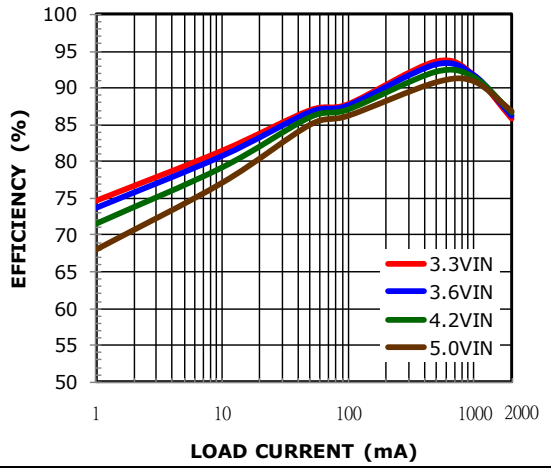

FIG.15 EFFICIENCY V.S. LOAD CURRENT

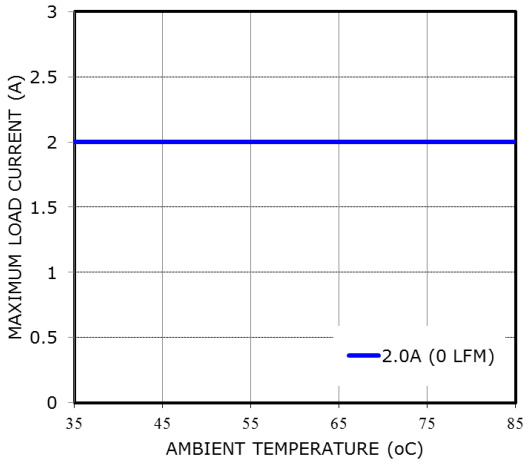

FIG.16 DE-RATING CURVE

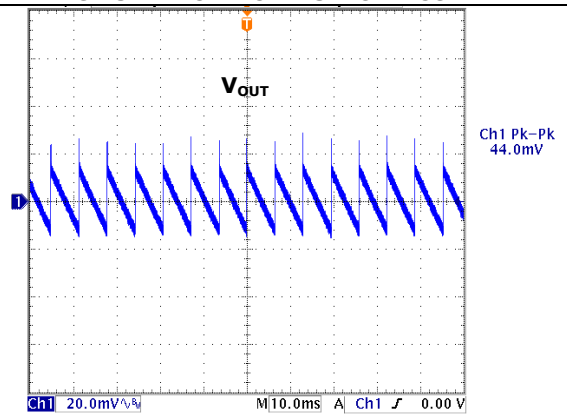

FIG.17 OUTPUT RIPPLE
(5VIN, IOUT=0A)

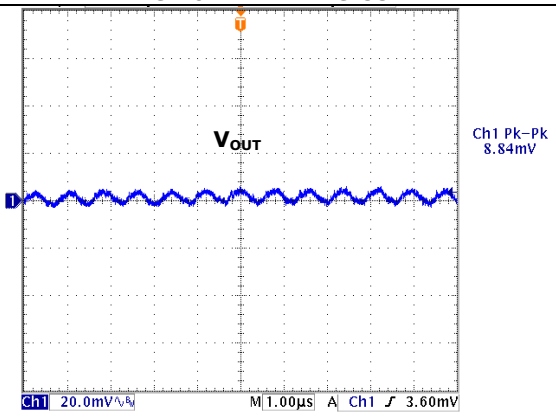

FIG.18 OUTPUT RIPPLE
(5VIN, IOUT=2A)

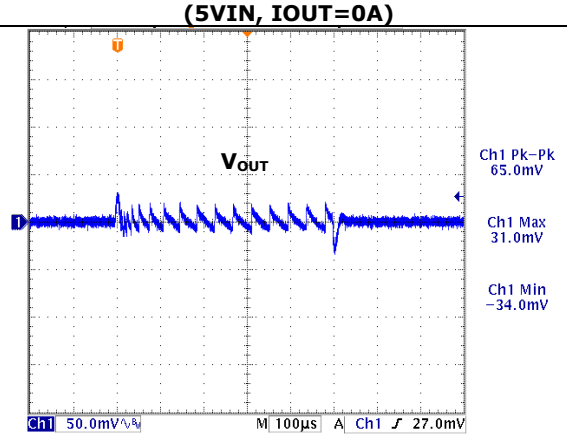

FIG.19 TRANSIENT RESPONSE
(5VIN, 0% to 100% LOAD STEP)

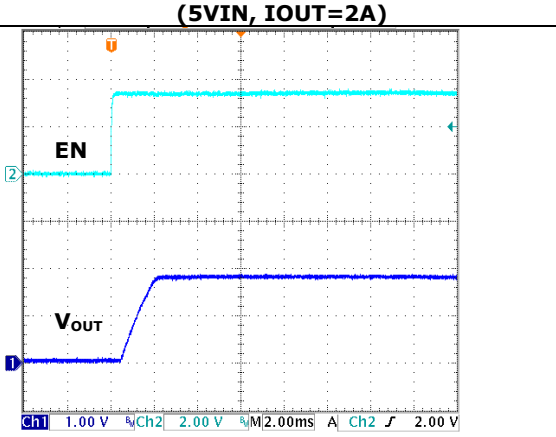

FIG.20 TURN-ON
(5VIN, IOUT=2A)

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2A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (2.5VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 76.2mm×76.2mm×1.6mm, 4 layers. The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.

The following figures provide the typical characteristic curves at 2.5Vout.

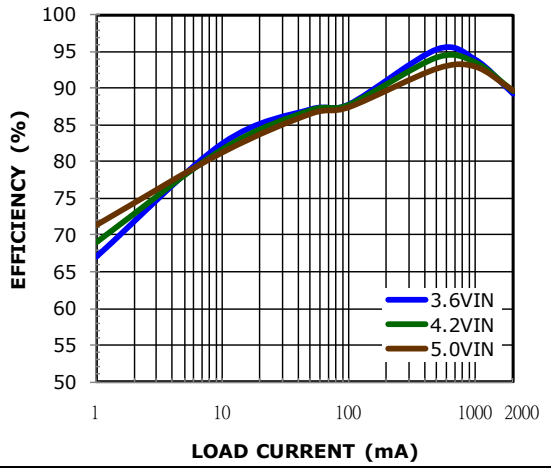

FIG.21 EFFICIENCY V.S. LOAD CURRENT

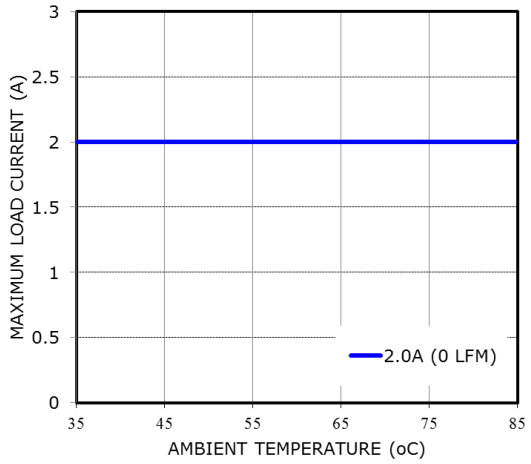

FIG.22 DE-RATING CURVE

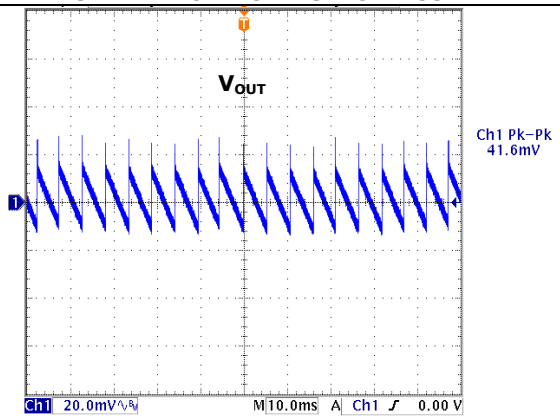

FIG.23 OUTPUT RIPPLE
(5VIN, IOUT=0A)

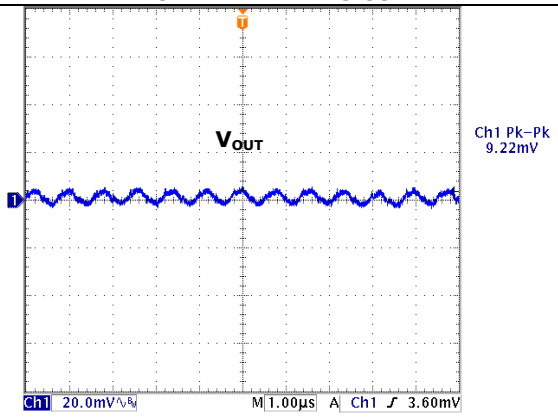

FIG.24 OUTPUT RIPPLE
(5VIN, IOUT=2A)

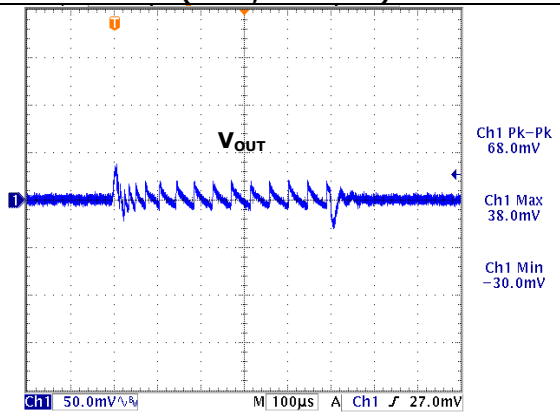

FIG.25 TRANSIENT RESPONSE
(5VIN, 0% to 100% LOAD STEP)

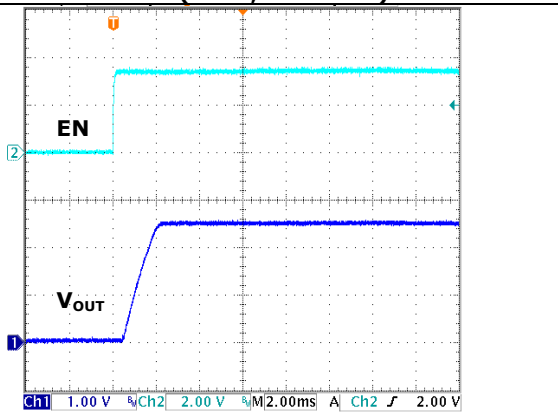

FIG.26 TURN-ON
(5VIN, IOUT=2A)

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2A, High Efficiency LDS Module

TYPICAL PERFORMANCE CHARACTERISTICS: (3.3VOUT)

Conditions: T_A = 25 ºC, unless otherwise specified. Test Board Information: 76.2mm×76.2mm×1.6mm, 4 layers.
The output ripple and transient response measurement is short loop probing and 20MegHz bandwidth limited.

The following figures provide the typical characteristic curves at 3.3Vout.

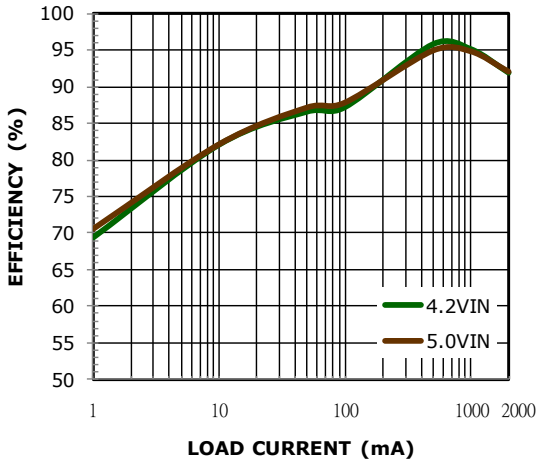

FIG.27 EFFICIENCY V.S. LOAD CURRENT

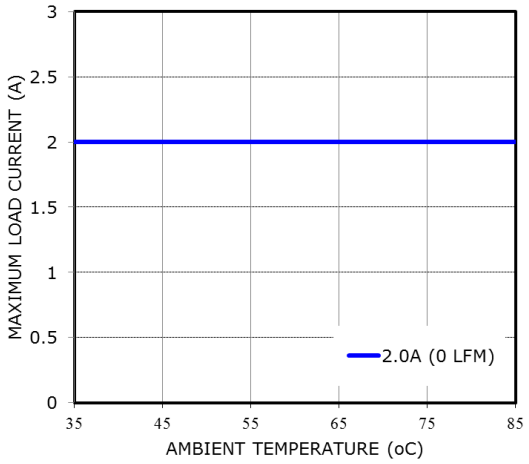

FIG.28 DE-RATING CURVE

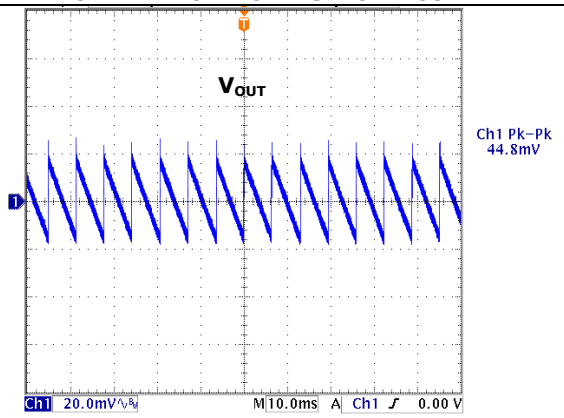

FIG.29 OUTPUT RIPPLE
(5VIN, IOUT=0A)

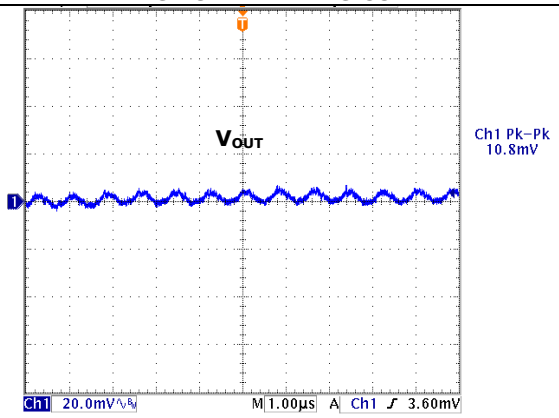

FIG.30 OUTPUT RIPPLE
(5VIN, IOUT=2A)

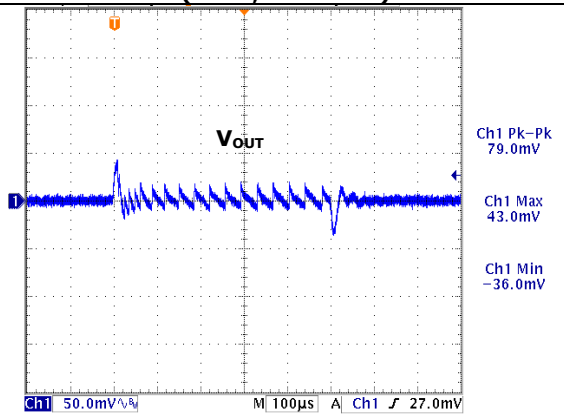

FIG.31 TRANSIENT RESPONSE
(5VIN, 0% to 100% LOAD STEP)

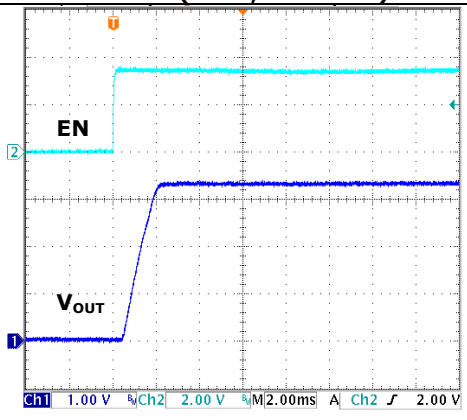

FIG.32 TURN-ON
(5VIN, IOUT=2A)

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2A, High Efficiency LDS Module

APPLICATIONS INFORMATION:

REFERENCE CIRCUIT FOR GENERAL APPLICATION:

The Figure 33 shows the module application schematics for input voltage +5V or +3.3V and turn on by input voltage directly through enable resistor (REN).

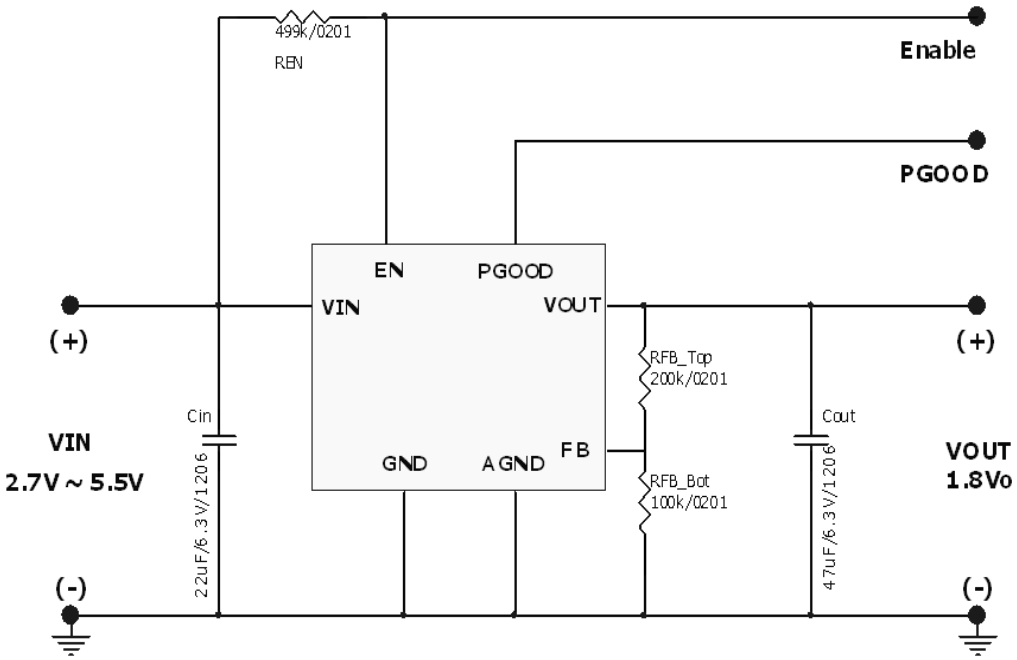

FIG.33 REFERENCE CIRCUIT FOR GENERAL APPLICATION

APPLICATIONS INFORMATION: (Cont.)

SAFETY CONSIDERATIONS:

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Fuses should also be used when there is the possibility of sustained input voltage reversal which is not current limited. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line. The installer must observe all relevant safety standards and regulations.

For safety agency approvals, install the converter in compliance with the end-user safety standard.

INPUT FILTERING:

The module should be connected to a low AC impedance source supply and a highly inductive source or line inductance can affect the stability of the module. An input capacitor must be placed directly to the input pin of the module, to minimize input ripple voltage and ensure module stability.

OUTPUT FILTERING:

To reduce output ripple and improve the dynamic response to as step load change, the additional capacitor at the output must be used. Low ESR polymer and ceramic capacitors are recommended to improve the output ripple and dynamic response of the module.

PROGRAMMING OUTPUT VOLTAGE:

The module has an internal 0.6V±2% reference voltage. The output voltage can be programed by the dividing resistance RFB which respects to FB pin and GND pin. The output voltage can be calculated as shown in Equation 1 and the resistor according to typical output voltage is shown in TABLE 1.

$$\mathrm{VOUT\,(V)} = 0.6 \times \left(1 + \frac{\mathrm{RFB\_top}}{\mathrm{RFB\_bot}}\right) \qquad \text{(EQ.1)}$$

Vout (V)	RFB_top (kΩ)	RFB_bot (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

TABLE.01 Resistor values for common output voltages

APPLICATIONS INFORMATION: (Cont.)

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 34.

1. The ground connection between pin 10 and 13 should be a solid ground plane under the module. It can be connected to one or more ground plane by using several Vias.
2. Keep the R_{FB_top} and R_{FB_bot} connection trace to the module pin 5 (FB) short.
3. Use large copper area for power path (VIN, VOUT, and GND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layers.

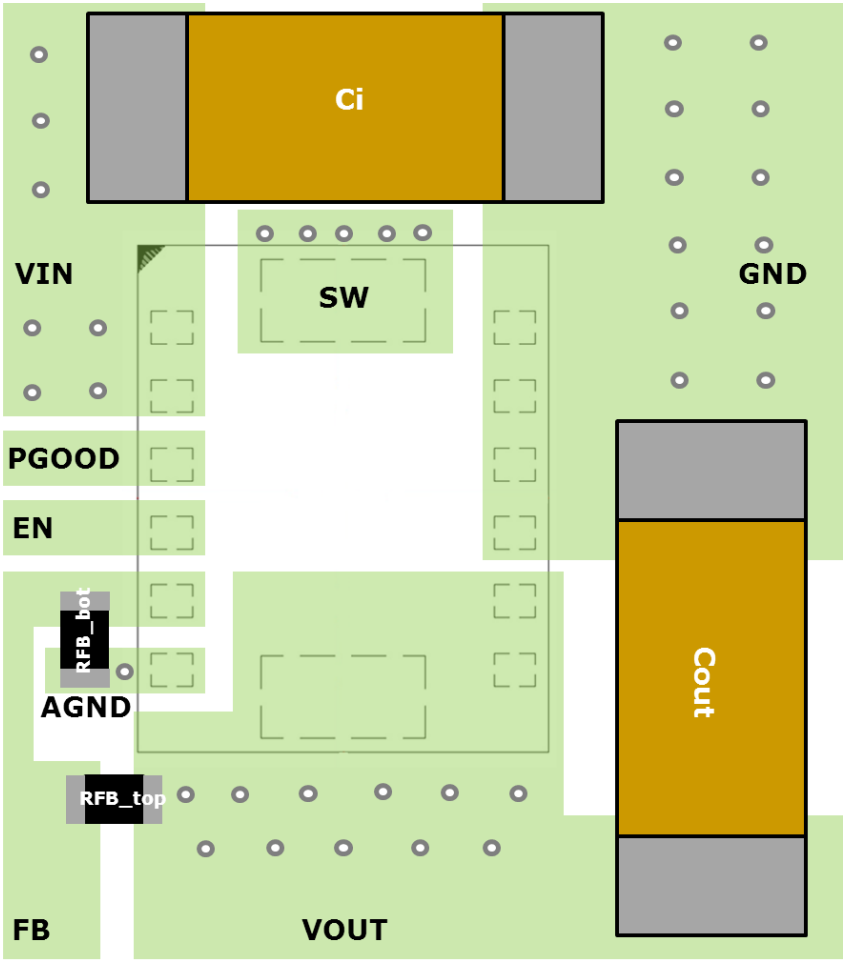

FIG.34 RECOMMENDATION LAYOUT (TOP LAYER)

APPLICATIONS INFORMATION: (Cont.)

Thermal Considerations:

All thermal testing condition is complied with JEDEC EIJ/JESD 51 Standards. Therefore, the test board size is 76.2mm×76.2mm×1.6mm with 4 layers. The case temperature of module sensing point is shown as Figure 35. Then Rth(j_{choke}-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The power module is designed for using when the case temperature is below 110°C regardless the change of output current, input/output voltage or ambient temperature.

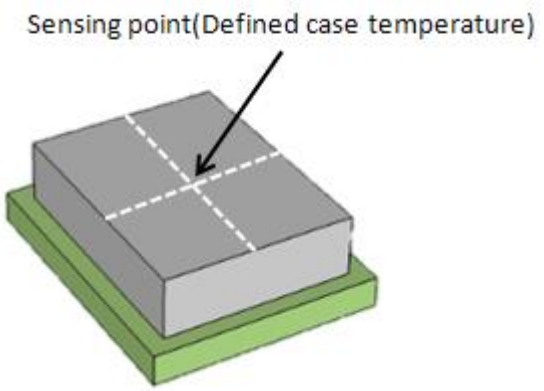

Figure 35. Case Temperature Sensing Point

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REFLOW PARAMETERS:

Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. Figure 9 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C, the ramp rate of temperature should be not more than 1.5°C/sec. The soak zone then occurs from 100°C to 180°C and should last for 90 to 120 seconds. Finally the temperature rises to 230°C to 245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.

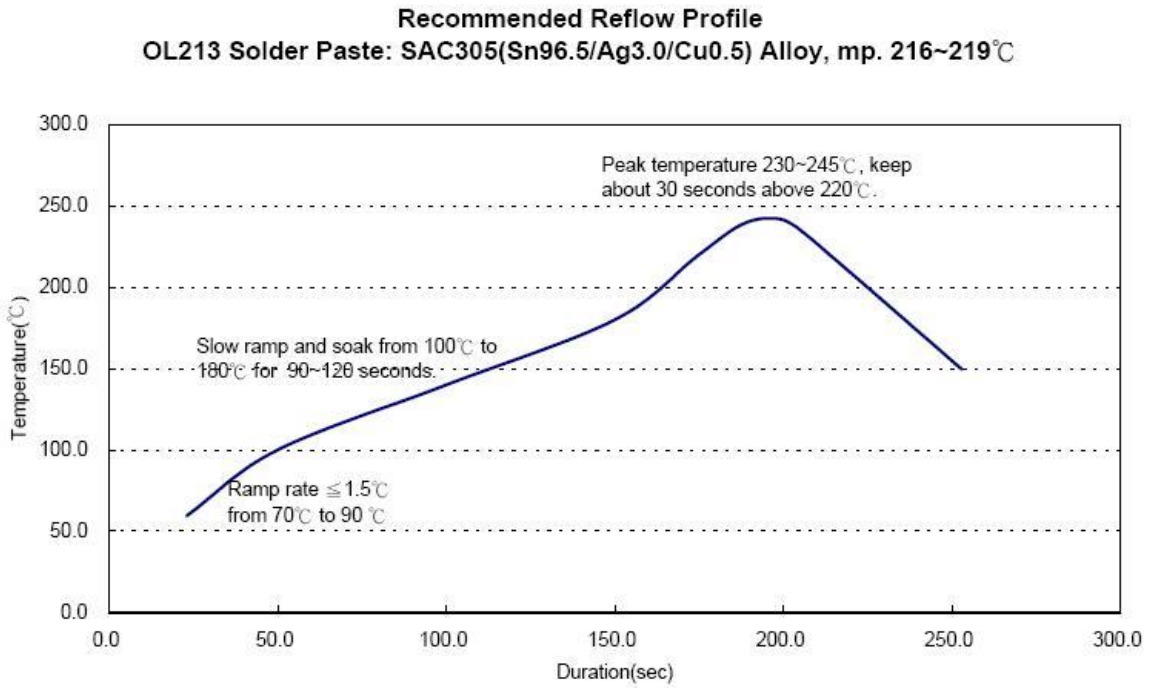

FIG.36 Recommendation Reflow Profile

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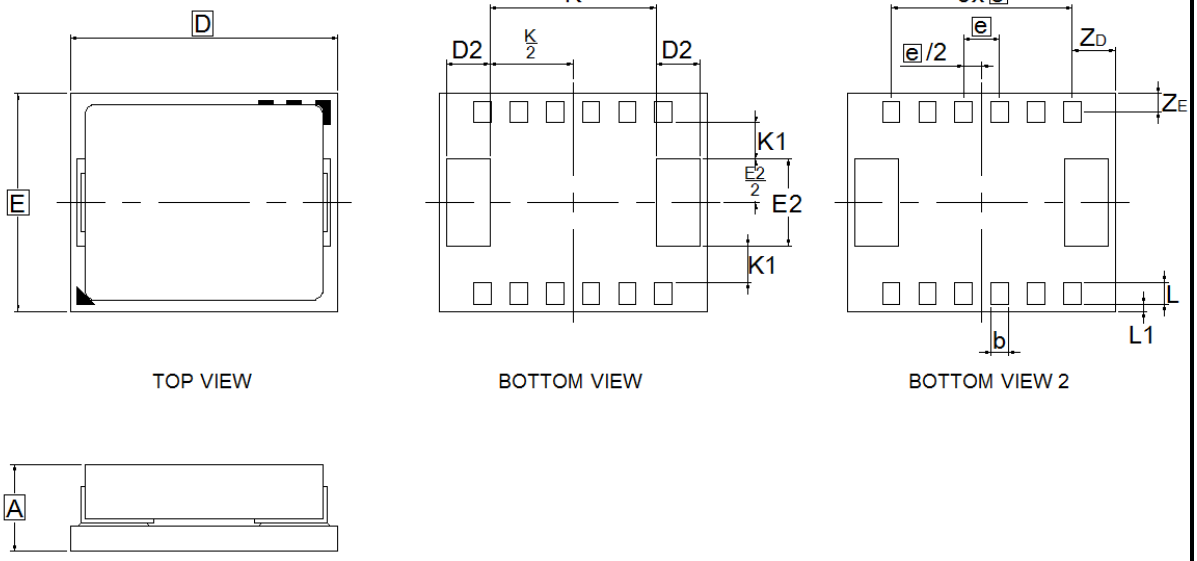
PACKAGE OUTLINE DRAWING:

Unit: mm



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.00	1.10	1.20
b	0.14	0.24	0.34
D	3.6	3.7	3.8
D2	0.5	0.6	0.7
E	2.9	3.0	3.1
E2	1.1	1.2	1.3
e	0.40	0.50	0.60
K	2.2	2.3	2.4
K1	0.4	0.5	0.6
L	0.2	0.3	0.4
L1	0	0.1	0.2
ZD	0.50	0.60	0.70
ZE	0.15	0.25	0.35

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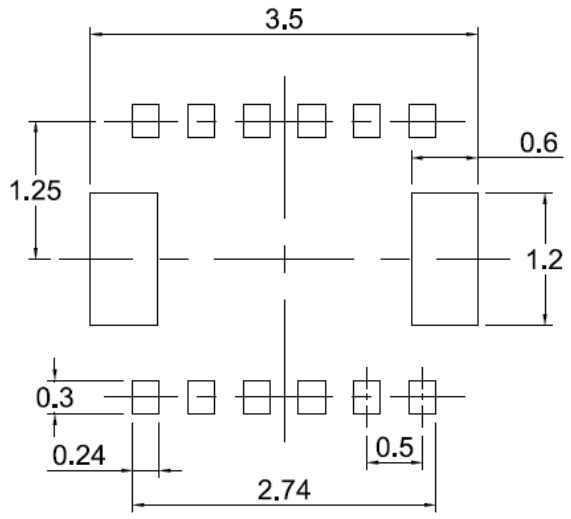
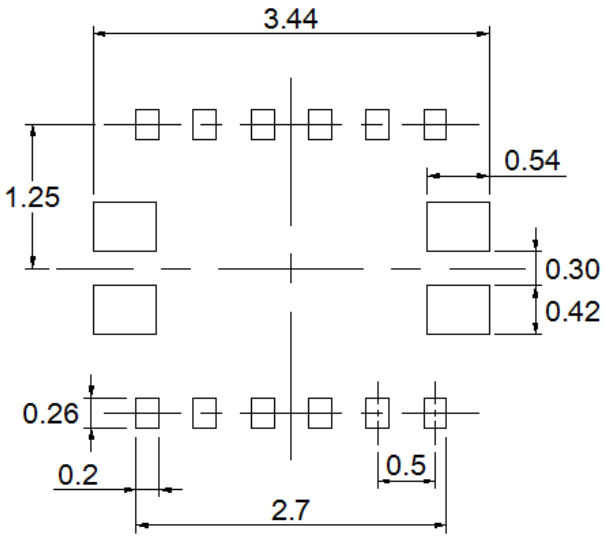
LAND PATTERN REFERENCE:

Unit: mm



RECOMMENDED LAND PATTERN



RECOMMENDED STENCIL PATTERN
BASED ON 130um THICK STENCIL

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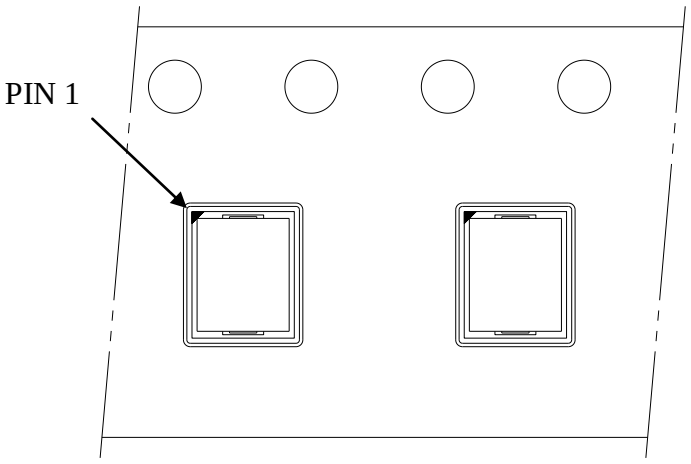
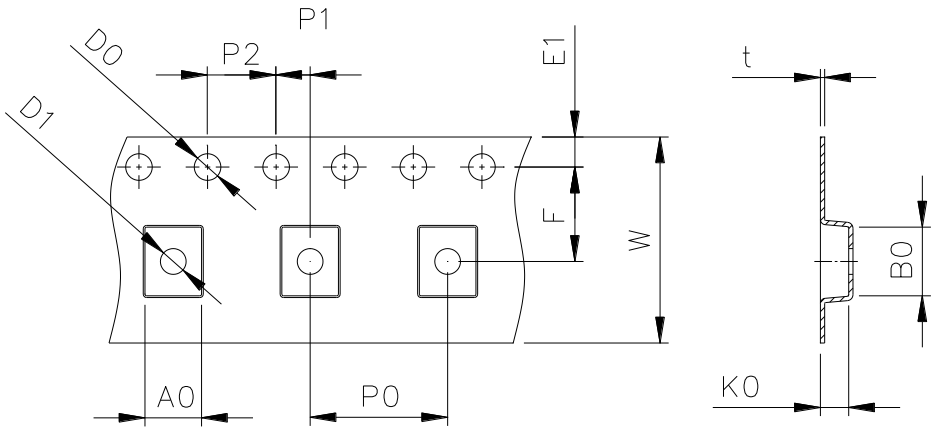
PACKING REFERENCE:

Unit: mm

Package In Tape Loading Orientation



Tape Dimension



A0	3.3 ± 0.10	E1	1.75 ± 0.10
B0	4.0 ± 0.10	K0	1.65 ± 0.10
F	5.50 ± 0.05	P0	8.00 ± 0.10
W	12.0 ± 0.30	P1	2.00 ± 0.05
D0	φ1.5 +0.10/-0.00	P2	4.00 ± 0.10
D1	φ1.50± 0.10	t	0.25 ± 0.1

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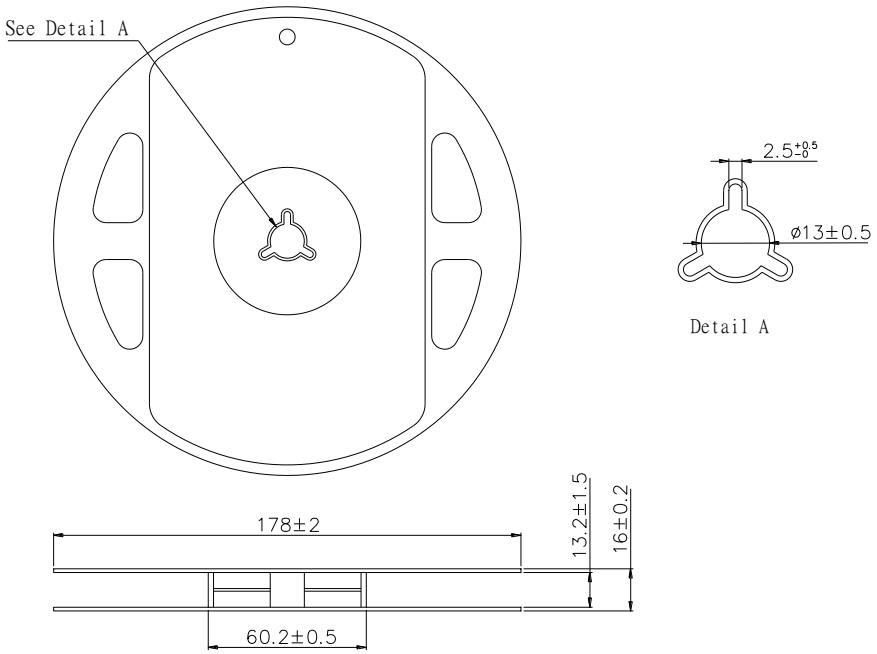
PACKING REFERENCE: (Cont.)

Unit: mm

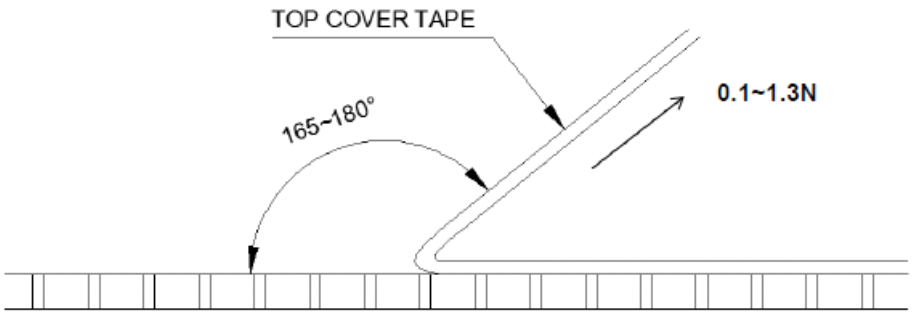
Reel Dimension



Peel Strength of Top Cover Tape

The peel speed shall be about 300mm/min.

The peel force of top cover tape shall be between 0.1N to 1.3N



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2A, High Efficiency LDS Module

REVERSION HISTORY:

Date	Revision	Changes
2013.12.06	00	Release the preliminary specification.
2014.01.08	01	Thermal de-rating updated. Thermal resistance Rth(j-a) updated. Packing reference revised.
2014.11.11	02	Release new part number.
2014.12.22	03	Update land pattern and reference layout.
2014.12.31	04	Update uPOL module to LDS module
2015.05.20	05	Update package outline drawing data.